AMENDMENTS TO THE CLAIMS

Please amend claim 9 as follows:

1. (Previously Presented) A source synchronous clocking system, comprising:
a source clock domain in a first network protocol layer, comprising:
a register having a first input for receiving a data signal, a second input for receiving a clock signal, and an output; and
a buffer having an input for receiving the clock signal and an output, said buffer generating a delay that is substantially equivalent to a delay through said register; and
a destination clock domain in a second network protocol layer, comprising:
a register having a first input and a second input, the first input of said register of said destination clock domain being coupled to the output of said register in the source clock domain.

2. (Previously Presented) The source synchronous clocking system of Claim 1 wherein said source clock domain comprises a first transmit clock domain in the first network protocol layer for transmitting the data and clock signals to the said destination clock domain that comprises a transmit clock domain in the second network protocol layer, said first network protocol layer comprising a link layer, said second network protocol layer comprising a PHY layer.

3. (Previously Presented) The source synchronous clocking system of Claim 1 wherein said source clock domain comprises a first receive domain said the first network protocol layer for transmitting data and clock signals to said destination clock that comprises a receive clock domain in said second network protocol layer, said first layer including a PHY layer, said second network protocol layer including a link layer.

4. (Original) The source synchronous clocking system of Claim 1 further comprising a delay circuit, coupled between said source clock domain and said destination clock domain, for introducing additional delay to the clock signal.

5. (Original) The source synchronous clocking system of Claim 1 further comprising a second buffer having an input coupled to the output of said delay circuit and an output coupled to said register in said destination clock domain.

6. (Original) The source synchronous clocking system of Claim 1 further comprising a serial termination circuit for absorbing a reflection generated by the data signal.

7. (Original) The source synchronous clocking system of Claim 1 further comprising a parallel termination circuit for absorbing a reflection generated by the data signal.

8. (Original) The source synchronous clocking system of Claim 5 wherein the clock signal generated from the output of the second buffer being connected to a clock input of in said destination clock domain.

9. (Currently Amended) A method for operating a source synchronous clocking system between a first layer and a second layer from a source clock, comprising:

receiving an input clock signal in a first clock domain in a first layer;

receiving an input data signal in the first clock domain in the first layer;

latching the input data signal in response to ~~by triggering the input data signal by~~ the input clock signal;

delaying the input clock signal by an amount that is equal to the delay in the latching; and

generating an output clock signal and an output data signal in the second clock domain in the second layer, the output clock signal and the output data signal being synchronized to each other.

10. (Original) The method of Claim 9 wherein the first layer comprises a link layer and the second layer comprises a PHY layer, the input clock and data signal being transferred from the link layer to the link layer.

11. (Original) The method of Claim 9 wherein the first layer comprises a PHY layer and the second layer comprises a link layer, the input clock and data signal being transferred from the PHY layer to the link layer.

12. (Cancelled)

13. (Cancelled)

14. (Previously Presented) A method for providing a clock input and a data input synchronously between a link layer and a PHY layer, the link layer including a transmit clock domain and a receive clock domain, the PHY layer including a transmit clock domain and a receive clock domain, comprising the steps of:

receiving the clock input;

receiving the data input;

transmitting the clock input to a latching device for triggering the data input;

sending the clock input through a buffer, the buffer having a delay which is equal to the delay through the latching device; and

generating an output data from the latching device that synchronizes with an output clock from the buffer.

15. (Original) The method of Claim 14 wherein the transmitting step comprises transmitting the clock input from a link layer to a PHY layer.

16. (Original) The method of Claim 14 wherein the transmitting step comprises transmitting the clock input from a PHY layer to a link layer.

17. (Original) The method of Claim 14 further comprising the step of merging the clock signal at eh PHY layer to a clock input at the PHY layer.

18. (Original) The method of Claim 14 further comprising the step of absorbing the reflection generated from the data input by serial termination.

19. (Original) The method of Claim 14 further comprising the step of absorbing the reflection generated from the data input by parallel termination.

20. (Original) The method of Claim 14 further comprising generating control signals of the data input, the control signals being multiplexed with the data input.